Disruptive Technologies

Marius Keown – Systems Engineer @ Arista Networks
Moore’s Law

- Dr Gordon E. Moore – Co-Founder of Intel
- Predicted in 1965 the doubling of components per integrated circuit every year
- In 1975 revised the forecast to doubling every 2 years
- Used for decades as the guide for the industry for new products
- Nothing like this in the history of mankind
Impact on Technology Industry

- Economic Impact – Performance and Cost
- Modern Computing
Moore’s Law and Networking

Why has Networking not kept up with Moore’s Law?

- CPUs: \(2X/2Y = 64X/12Y\)
- WAN Routers: \(4X/12Y\)
Three main problems

- **Moore’s Law applies to Transistors, not Speed**
  - Transistor count is doubling every 2 years
  - Transistor speed is only increasing slowly

- **Number of I/O pins per package basically fixed**
  - Limited by the area and package technology
  - Only improvement is increased I/O speed

- **Bandwidth ultimately limited by I/O capacity**
  - Throughput per chip = # IO Pins x Speed/IO
  - No matter how many transistors are on-chip
Number of SERDES per Package

Modest Increase in 12 Years
Maximum Throughput per Chip

Tbps

2002 2006 2010 2014

10X in 12 Years
Moore’s Law and Networking

Maximum Throughput per Chip

- LAN 1GbE to 10GbE: 10X/12Y
- WAN Routers: 4X/12Y
- CPUs: 2X/2Y = 64X/12Y

Why has Networking not kept up with Moore’s Law?

10X in 12 Years
Network Switching Industry

Network ASIC performance has not increased like CPU performance.

In a 12 year span:
• Network ASIC increased: 10x
• CPU perf has increased: 64x
• Investment vs. ROI
• Low speeds, low port density, high power consumption
• Long and slow development cycle
• Inflexible to market changes

ASIC = Application Specific Integrated Circuit
• Top down design, independent of the layout
• Network Vendor focusing on the functionality not the implementation
• ASIC supplier does the physical implementation
• Difficult to achieve high clock rates and scale

Full Custom design flow
• Bottom up approach, chip vendor focus on potential implementation
• Chip design starts with the clock rate objective
• Data paths optimize to achieve the clock rates
• Only way to achieve high clock rates

Only the Full custom Chip will allow us to scale for the future.
Merchant Silicon 64-ports 10G Switch Chip

- SERDES (Ports)
- Buffer Memory (~10MB)
- L2 (MAC) hash table
- Forwarding logic
- TCAM (ACL etc.)
- L3 (LPM) m-trie
Port Density on Merchant Silicon

- Broadcom Trident 2
  - 128 x 10G
  - 32 x 40G

- Broadcom Tomahawk
  - 32 x 100G
  - 128 x 25G

- Broadcom Jericho
  - 6 x 100G, but with Big Buffers and large routing tables
## Advantages of Merchant Silicon

- More ports per chip, increased throughput
- More room for additional logic/processing/functionality
- Less Chips:
  - Increased reliability, reduced complexity
  - Reduced latency (fewer chip crossing)
  - Consume less power (less chips less power draw)

### Custom Design vs. ASIC Design

<table>
<thead>
<tr>
<th>Custom Design: 1 Chip</th>
<th>ASIC Design: 10 Chips</th>
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<tbody>
<tr>
<td><img src="image1.png" alt="Custom Design" /></td>
<td><img src="image2.png" alt="ASIC Design" /></td>
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- Merchants’ full custom chips are now on Moore’s Law growth rate
- ASIC designs are NOT on Moore’s Law growth
Merchant Silicon for SP
Hyper Connected World

We are in an age of exponential growth

Sources: Cisco, Gartner, CMA Research, EdgeConneX
Over-the-Top Video
Mobility
SP Market Dynamics
NFV
Hyper Scale DC
Emerging SP Challenge and Opportunity
SP Networks Transformation

**Requirement**

- Urgent Network C/O-EX Optimization
- Operational Efficiency
- Improved Revenue Stream

**APPROACH**

- Sustainable OPEX compression
  - Reliable and Cost Optimized Hardware
  - NFV
- Operational re-engineering
  - Operational Automation Programmable Network
- Network Re-architecture
  - Re-Architect for the Least Common Denominator
Bringing Merchant Silicon to the WAN Edge

WAN Edge (CE) routers represent highest CapEx investment in infrastructure today

Challenges:
• Many niche features
• Full internet routing table in hardware
Less Than Half the Power Consumption

• Half the power compared to closest competitor
• >6X more power efficient than legacy
Merchant Silicon vs. Legacy Router Price

- Legacy Routing Platforms heavy on features, power, and price
- Expect new Routing switch platforms to disrupt installed base
Merchant Silicon for SP
Use Cases
1: DC CORE NEEDS A SPINE
2: Internet Peering – Evolution to Content Peering
3: Cloud and WAN Segment Routing

Legacy TE
- Complex, State heavy
- Hop by hop Traffic Engineering
- Path computation
- MPLS TE signaling
- IGP, BGP

Segment Routing
- Intelligent Source Routing
- Globally optimized traffic engineering
- Path computation
- Programmatic API's
- IGP, BGP - Segment Routing
- Reduces complexity
- Improves scale

Software Driven Control

DC1

DC2
4: Telco Transformation - Service Provider NFV

**SP Service Edge Evolution**

- Time to Market for new Services Increase
- Over The Top Traffic Increase
- Reliance on expensive HW Service Edge Routers

**Next Gen Telco NFV Cloud**

- Software Strategy - Orchestration, Service instantiation
- Universal Cloud Network Leaf-Spine Architecture
- Virtualize and Scale Out

SDN Controller

Deep Buffer Leaf-Spine Architecture
Summary

- Following Moore’s Law
- Higher Port Density
- Lower Price per Port
- Lower Power Consumption
Thank You